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1 **A comprehensive layout methodology and layout-specific circuit analyses for three-dimensional integrated circuits**
Alam, S.M.; Troxel, D.E.; Thompson, C.V.;
Quality Electronic Design, 2002. Proceedings. International Symposium on , 1
March 2002
Pages:246 - 251

[Abstract] [PDF Full-Text (466 KB)] **IEEE CNF**

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2 **A manufacturable embedded fluorinated SiO_2 for advanced 0.25 μm CMOS VLSI multilevel interconnect applications**
Pai, C.S.; Velaga, A.N.; Lindenberger, W.S.; Lai, W.Y.-C.; Cheung, K.P.; Baur F.H.; Chang, C.P.; Liu, C.T.; Liu, R.; Diodato, P.W.; Colonell, J.I.; Vaidya, H.; Vitkavage, S.C.; Clemens, J.T.; Tsubokura, F.;
Interconnect Technology Conference, 1998. Proceedings of the IEEE 1998 International , 1-3 June 1998
Pages:39 - 41

[Abstract] [PDF Full-Text (520 KB)] **IEEE CNF**

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3 **Automatic generation of symbolic cells from a net-list description**
Costa, R.; Curatelli, F.; Caviglia, D.D.;
CompEuro '89., 'VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks', Proceedings. , 8-12 May 1989
Pages:5/35 - 5/39

[Abstract] [PDF Full-Text (360 KB)] **IEEE CNF**

A Comprehensive Layout Methodology and Layout-Specific Circuit Analyses for Three-Dimensional Integrated Circuits

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Abstract

In this paper, we describe a comprehensive layout methodology for bonded three-dimensional integrated circuits (3D ICs). In bonded 3D integration technology, parts of a circuit are fabricated on different wafers, and then, the wafers are bonded with a glue layer of Cu or polymer based adhesive. Using our layout methodology, designers can layout such 3D circuits with necessary information on inter-wafer via/contact and orientation of each wafer embedded in the layout. We have implemented the layout methodology in 3DMagic. Availability of 3DMagic has led to interesting research with a wide range of layout-specific circuit analyses, from performance comparison of 2D and 3D circuits to layout-specific reliability analyses in 3D circuits. Using 3DMagic, researchers have designed and simulated an 8-bit encryption processor mapped into 2D and 3D FPGA layouts. Moreover, the layout methodology is an essential element of our ongoing research for the framework of a novel Reliability Computer Aided Design tool, ERNI-3D.

1. Introduction

Recent development in technology has enabled the fabrication of a single chip with multiple device-interconnect layers (wafers) stacked on each other. This novel approach is commonly referred to as the 3D integration of ICs. The main idea behind 3D integration is to have multiple device layers in the third plane (z plane) and lower the interconnect length by connecting them vertically. This has been accomplished by bonding multiple wafers fabricated with different or similar technology as well as by fabricating multiple device (CMOS) layers on the same wafer [1-3]. The developed layout methodology enables layout of individual device-interconnect layer keeping in mind the position and orientation of the vertical/3D contacts. The methodology can be easily incorporated into existing IC layout tools. The layout methodology is also an essential element of a reliability analysis tool, ERNI-3D. ERNI-3D is a technology-generic tool for reliability analyses associated with electromigration, 3D bonding, and joule heating in 3D circuits.

2. A simple 3D Integrated Circuit (3D IC)

The Wafer Bonding technology with Cu/Ta at 400° C has shown promise for successful 3D integration with two or more device layers [1]. In this technology, each device-interconnect layer is fabricated separately on different wafers with same or different technologies, and then the wafers are bonded with each other with a bonding layer of Cu. The wafers are electrically interconnected using high aspect ratio vias or contacts. When the bonding is complete, 3D ICs have vertical interconnects of significantly higher length than vias or contacts in conventional or 2D integration of ICs. Moreover, the 3D circuits fabricated with wafer-bonding technology have two different types of vertical interconnects as shown in figure 1. The inter-wafer vias connect multiple interconnect trees in different wafers. And at the bonding surface, the adjacent metallization layers from two wafers can also be connected with vertical Cu lines. The vertical Cu lines create a new type of trees, referred to as a "3D tree", which expands between two different wafers in a 3D circuit.

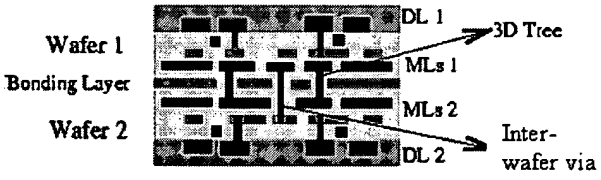

Figure 1. Cross-section a 3D IC. Here DL and MLs correspond to device and metal layers, respectively.

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3. Inter-wafer vias in 3D ICs

In order to facilitate the layout of 3D ICs, all types of inter-wafer vias or contacts are generalized into three major categories. Figure 2 shows the three categories of contacts along with their connectivity in a wafer. The three categories of vias are sufficient for defining almost all types of interconnection between wafers in 3D ICs. A detailed description of each category follows.

3.1. Connected-to-top via

This type of via connects a metal layer to a 3D contact point at the top[1] of a wafer. In figure 2, it is connected with Metal2, the topmost metallization layer of this particular wafer. The connected-to-top via can also connect other metal layers, such as Metal1 or Metal3 to a 3D contact point at the top. When two wafers are bonded on front-to-front, as shown in figure 1, a 3D tree is formed if the connected-to-top type vias of the topmost metal layers from the two wafers share the same 3D contact point at the bonding surface.

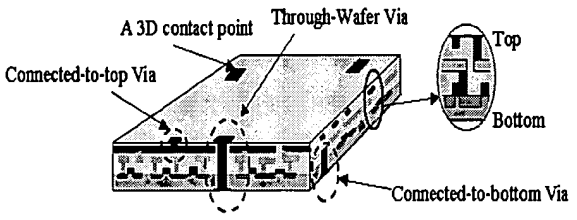


Figure 2. Different types of via/contact for 3D ICs.

3.2. Connected-to-bottom via

The connected-to-bottom type via extends between a metal layer and a 3D contact point at the bottom[2] of a wafer. In figure 2, a connected-to-bottom via connects Metal1 to a 3D contact point. When two wafers are bonded on back-to-front, a 3D tree is formed if a connected-to-bottom via from the top wafer and a connected-to-top via of the topmost metal layer from the bottom wafer share the same 3D contact point. Similarly, two connected-to-bottom type vias of different wafers with the same 3D contact point can also create a 3D tree when they are bonded on back-to-back.

3.3. Through-wafer via

Through-wafer via extends through the whole wafer without being electrically connected to any interconnect or active layer of the wafer. This type of via is particularly useful when more than two wafers are bonded to create a 3D IC. For example, in a three-wafer 3D circuit, an interconnect layer from the top wafer can be connected with that of the bottom wafer through a through-wafer via of the middle wafer. Moreover, Cu filled through-wafer vias can be designed as heat conductors to overcome the effect of increased Joule heating in a 3D IC. To represent a through-wafer via that is also electrically connected to an interconnect layer in a wafer, designer can add both connected-to-top and connected-to-bottom vias at the same position on that interconnect layer.

4. Implementation in Magic (3DMagic)

Magic is an interactive VLSI circuit layout editor developed at UC Berkeley [4]. It is widely used within the academic community. Moreover, it's well-documented source code and wide variety of features make it an excellent vehicle with which to conduct VLSI and CAD research. In order to implement the 3D IC layout methodology in Magic, we have developed a new technology (scmos3D.tech26) file to support all the new layers and inter-wafer vias. Several entries for display styles are also added in the file, mos.7bit.dstyle5 or mos.24bit.dstyle5. Since Magic is a technology independent layout editing tool, a 3D circuit can be designed on any Magic (version 6.4 or higher) with the display style file installed in the proper path and technology file specified with the -Ttechfile flag in the command line.

4.1. Graphical User Interface

Magic consists primarily of an internal data-structure representation of a 2D layout with a graphical user interface (GUI) to manipulate and view a circuit design. However, Magic also supports viewing multiple layouts on different windows and editing a layout on the edit window. Using this feature, the layout of different wafers in a 3D circuit can be done on different windows with new abstract layers (discussed in the next section) to specify the inter-wafer vias. The major issue with this approach is the alignment of different layouts and inter-wafer vias with the shared 3D contact points.

[1] Both "top" and "front" refer to metal side (opposite of the Si substrate side) of the wafer.
[2] Both ``bottom" and ``back" refer to the Si substrate side of the wafer.

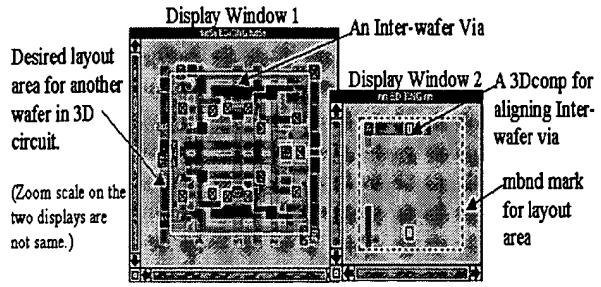


Figure 3. Graphical User Interface support for 3D IC layout in 3Dmagic.

The alignment issue has been resolved by introducing two area markers, mainboundry or mbnd for specifying layout size, and 3Dcontactpoint or 3Dconp for specifying the positions of inter-wafer vias. Figure 3 shows the usage of the area markers. In Display Window 1, one layer of a 3D circuit has been designed with proper abstract layers indicating the inter-wafer vias. The positions of inter-wafer vias and desired layout area for the second wafer/layer are also marked in Display Window 1. Now, the 3Dcontactpoints and mainboundry are retrieved in Display Window 2 at the corresponding positions. Further layout can be done on Display Window 2 with respect to the area markers to design second wafer/layer of the 3D circuit.

In order to automate the detection and placement of the area markers, a Magic feature, called "feedback" can be used. Table 1 shows the flow of commands and corresponding descriptions for making 3D layouts using the "feedback" feature. A 3D circuit laid out in such a way will have multiple files.

Table 1. Alignment of 3D layouts using "feedback".

Command	Description
in Display Window 1	
feedback add mbnd outline	Adds the main boundry mark for 3D layouts
feedback add iwvia1	Adds the inter-wafer via mark named iwvia1
....	Add more inter-wafer via marks similarly
feedback save afile	Saves all the area markers in file "afile"
in Display Window 2	
source afile	Paints all the area markers from file "afile". Corresponding name and style, such as outline, diagonal-cross, etc., of the area markers are also reserved.

4.2. Abstract layers

Abstract layers are the boxes in color that are drawn on the edit window to represent a particular mask layer, such as metal1, metal2, poly, ndiffusion, and so on. These layers are defined in the technology file. Two abstract layers are added as the connected-to-top via; Metal2_top_contact or m2topc, and Metal3_top_contact or m3topc, connecting metal2 and metal3 to a 3D contact point at the top, respectively. A connected-to-top via from metal1 is not defined, since in a scmos process with three levels of metal (supported by the technology file), circuits with only one metal layer are very unusual.

Similarly for the connected-to-bottom category of vias, the two new abstract layers are Poly_bottom_contact or pbcon, and Metal1_bottom_contact or m1bcon. Poly_bottom_contact directly connects poly1 with a 3D contact point at the bottom of a wafer. However, in order to connect Metal1 with a 3D contact point at the bottom, it is necessary to paint Poly_bottom_contact and Metal1_bottom_contact on top of each other in any order. The scheme in the current technology files only allows contacts for at most three layers together, and metal1 and 3D contact point at the bottom layer are two layers apart.

Painting the 3D contacts will automatically create the internal image of the corresponding 3D contact point at either the topmost or bottommost layer. Proper connectivity information is also added in the technology file to enable the built-in hierarchical circuit extractor successfully extract each layout of a 3D circuit. In the "drc" (Design Rule Checker) section of the technology file, some preliminary design rules are defined in terms of lambda (λ). However, depending on the process, these rules may vary and a designer may need to observe absolute micron rule for the contacts. Finally, an abstract layer named through-wafer via or twv has been defined to indicate an extension through the whole wafer.

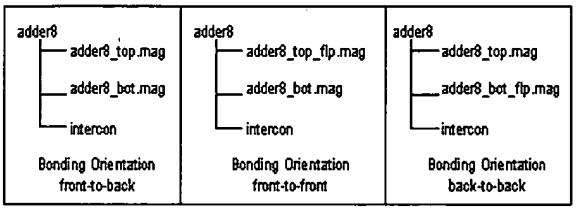
4.3. Strategy for layout management

A completely laid out 3D circuit in Magic will consist of multiple files; two or more layout files, of format .mag, for each wafer and one or more text files[3] containing the area markers. These files can be easily managed using a simple directory scheme. For example, all the files for a 3D Adder laid out in two wafers can be stored under a directory named *adder8*. In that directory, the two layout files, *adder8_top.mag* and *adder8_bot.mag*, and one text file for the 3D area markers, *intercon*, are stored. The suffix *_top* indicates that the corresponding layout is for the top wafer in the

[3] These text files are created with "feedback save afile" command.

3D stack, and similarly *_bot* indicates a layout for the bottom wafer. By default, the wafers are not flipped in the 3D stack. Therefore, to indicate that a particular layout is for a wafer that is also flipped, another suffix *_flp* is required. Table 2 shows the orientations with corresponding file structures.

Table 2. Layout-file structures for different orientations.



Thus, a designer can incorporate necessary information on the orientation of wafers for the 3D wafer bonding process and also add inter-wafer vias accordingly. The layout management scheme can be easily extended for 3D circuits with more than two wafers by indicating the middle wafers with different suffix, such as *_md1*, *_md2*, etc. starting from the top.

4.4. Circuit extraction and verification

Circuit extraction and verification are integral parts of CAD tools. Magic can extract circuits from layouts with extraction parameters retrieved from the technology file. To support circuit extraction in the initial version of 3DMagic, all the layouts of a 3D circuit are dumped into a single layout cell, and then extracted with the command ":extract all". The 3D connections between layouts are automatically done if the same label is used (using ":label") for inter-wafer vias of different layouts that requires to be connected. The extraction process creates a file with an extension, .ext, from the layouts. A spice netlist can be derived for the .ext file and simulated with HSpice or Spice with proper input vector for functional verification and other analyses.

5. Implication of the methodology

The need for standardization of CAD methodologies for 3D ICs is critical as the topic of 3D integration is receiving more and more attention in both the academia and industry. 3DMagic, the version of Magic with 3D layout capabilities, is available for the users of MIT's academic computing facility, Athena. Several researchers have used 3DMagic for a research project investigating the advantages of 3D integration. Performance comparison of 2D and 3D FPGAs is an outcome of such a project [5]. As a part of our ongoing reliability analyses work, we have developed a novel layout-specific reliability tool, ERNI-3D, for 3D ICs. Reliability of bonded 3D circuits is an area yet to be explored and the layout methodology has added another dimension to facilitate our research.

6. Layout-specific performance analyses of FPGAs

Field Programmable Gate Arrays (FPGAs) are reconfigurable chips that can implement arbitrary logic. However, this flexibility is achieved at the cost of low resource utilization, routing congestion, and high interconnect delay. 3D integration can alleviate some of these problems by mapping the configurable logic blocks into two or more layers/wafers and connecting them with shorter vertical wires.

6.1. Architecture of 2D and 3D

An 8-bit encryption processor was implemented in both 2D and 3D FPGAs by laying out the circuits using Magic and 3DMagic [5]. The 2D FPGA has 96 (16x6) blocks of RLBs (Routing and Logic Blocks) in a single layout and the 3D version has a slightly higher number (112) of RLBs (to facilitate routing) in two layouts. The functional unit in RLB consists of pass-transistor based logic circuitry and the eight control bits are fed from value stored in a register.

Triptych, the 2D architecture investigated, is a sea-of-gates type structure made from an array of RLBs instead of conventional configurable logic blocks [6]. The RLBs can be configured to implement a logic function as well as to act as a signal router. The 3D FPGA architecture, Rothko, was proposed by Northeastern University [7] and is directly based on Triptych. In Rothko, the sea-of-gates structure is extended to multiple layers or wafers. The implementation of 8-bit encryption processor has two layers in the 3D stack. The upper layer is dedicated almost exclusively for routing; whereas, the lower layer is used primarily for computation.

6.2. Result of simulation

Spice netlists were extracted from the layout of 2D and 3D FPGAs and simulated using PowerMill[4]. Both circuits were simulated with parameters for .30μm technology with a power supply of 3V. Table 3 shows the comparison of some performance parameters. Figure 4 shows simulation for critical path delay in the 2D and 3D FPGAs.

[4] PowerMill is a high-speed circuit simulator available from Synopsis.

Table 3. Performance of 2D and 3D FPGAs.

	Critical path delay	RLBs used	Power
2D	62ns	70.8%	2.59mW
3D	53ns	85.7%	2.77mW

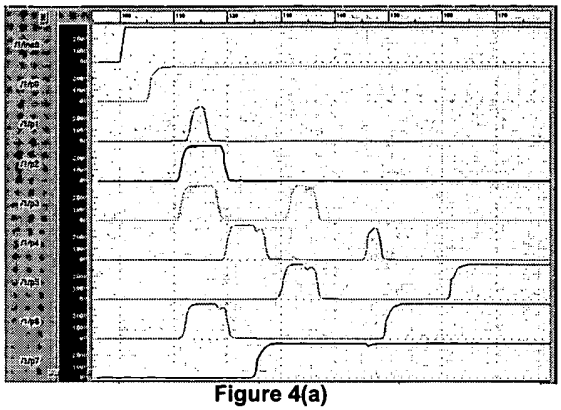


Figure 4(a)

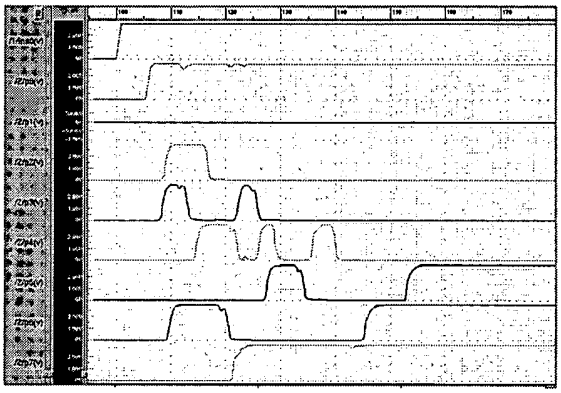


Figure 4(b)

Figure 4. Simulation for critical path delay of (a) 2D and (b) 3D FPGAs in PowerMill. The first waveform shows that the input signal transitions at 100ns, while the rest of the waveforms are 8-bit output. The outputs settle to their final values at 153ns and 162ns in 3D and 2D respectively.

6.3. Discussion of results

Table 3 shows some advantages in the 3D FPGA even though the improvements do not match the maximum expectation from theoretical analysis. The improvement in interconnect delay is only 15% contrary to around 53% estimated from system-level modeling analysis [8,9]. The modeling analysis does not consider actual circuit being implemented, rather it assumes a standard FPGA architecture and straightforward extension of switch boxes to 3D technology. Therefore, the actual improvement varies from the ideal case based on circuit design and implementation details in the architecture. The percentages of used RLBs show that the 3D design has better resource utilization that its 2D counterpart.

Total power dissipation is in fact higher for the 3D FPGA in terms of absolute value. More RLBs are in operation in the 3D design, and the implementation of functional block in the RLB has nMOS pass-transistor based logic where output from the pass-transistors feed into inverters. This particular implementation increased static power consumption (30% of the total power in the 3D design). A more useful metric is the difference in power dissipation due to interconnect. Simulation shows that interconnect for 3D consumes 5% less power than 2D.

The 3D FPGA design can be further improved (by using a circuit with no static power dissipation, or using different mapping/architecture) to decrease power dissipation and interconnect delay. Moreover, the 8-bit encryption processor may not have enough complexity to fully achieve the gains of 3D integration. Therefore, research and experiment with actual circuit implementations are equally important to fully harness the advantages of a new technology. Availability of CAD methodologies for 3D integration technology and tools, such as 3DMagic, can set such research direction.

7. Layout-specific reliability analyses

Although there has been some research on the impact of 3D integration on chip size, interconnect delay, and overall system performance, not much is known about the reliability issues in 3D integrated circuits. We have developed a framework for reliability analyses in 3D circuits with a novel Reliability Computer Aided Design (RCAD) tool, ERNI-3D. Using ERNI-3D, circuit designers can get interactive feedback on the reliability of their circuits associated with electromigration, 3D bonding, and joule heating. Moreover, addressing the reliability issues at the circuit layout level makes our approach unique.

ERNI-3D parses 3D circuit layouts, and extracts both conventional and 3D interconnect trees. It employs the Hierarchical Reliability Analysis approach, and filters out a group of immortal trees (trees that will never fail) using their current-density length products [10, 11]. After the filtering process, stringent reliability models are applied to the remaining interconnect trees for computing their median and mean time to failures. Finally, multiple time to failures are combined using a joint probability distribution to report a single reliability figure for the whole chip. Figure 5 shows a screen shot of ERNI-3D working on a 3D 8-bit Adder layout.

The initial version of ERNI-3D treats 3D circuits with two wafers or device-interconnect layers in the stack. However, data-structures and algorithms in the tool are generic enough to make it compatible with 3D circuits

with more than two device-interconnect layers, and to allow incorporation of more sophisticated reliability models (specially 3D bonds and joule heating models as they are under development) in the future.

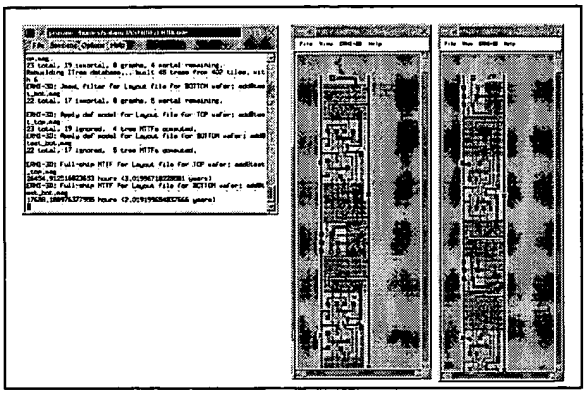


Figure 5. Graphical User Interface of ERNI-3D with a 2-wafer 3D 8-bit Adder layout.

8. Conclusion

A comprehensive layout methodology for bonded 3D integrated circuit is proposed and implemented in 3DMagic. The layout methodology can be incorporated into any existing CAD tools with minimal changes and yet it is powerful enough for design of a 3D circuit of any complexity. Using 3DMagic, researchers have designed and simulated an 8-bit encryption processor mapped into 2D and 3D FPGAs to investigate the improvements in key performance parameters. The 3D FPGA demonstrates a performance improvement, however, not at the same scale as expected from empirical modeling. Apparently, performance improvement is dependent on actual circuit implementation and the layout methodology presented here will allow further research with different circuit topologies to fully harness the advantages of 3D integration. Availability of the layout methodology and 3D circuit layouts has also started a new research area for exploring the reliability issues in bonded 3D integration technology. We have developed a novel RCAD tool, ERNI-3D for reliability analyses associated with electromigration, 3D bonding, and joule heating. The initial version of ERNI-3D treats 3D circuit layouts in two wafers and applies electromigration analysis in both conventional and 3D interconnect. It has the infrastructure to incorporate more sophisticated reliability models as they are developed.

9. Acknowledgements

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